FIN 404 PCT

Abstract

Arrangement of contact areas and test areas on patterned semiconductor chips

The invention relates to an arrangement of contact areas (1) and test areas (2) on patterned semiconductor chips (3). The contact areas (1) and the test areas (2) are electrically connected to one another via a conduction web (4). Whereas the contact areas (1) are arranged in a first region (5), which has no components of an integrated circuit, the test areas (2) lie in a second region (7) of the top side of the semiconductor chip (3), which region has components (6) of an integrated circuit.

[figure 1]